# AP6606C

## *USB Type-C and PD Charging Controller*

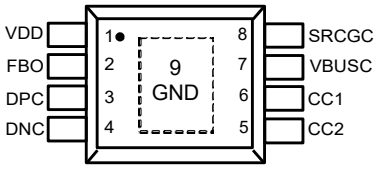
## Description

The AP6606C is a simplified USB Power Delivery 3.0 protocol controller. It also integrated functions for HiSilicon Fast Charging Protocol (FCP) and Qualcomm Quick Charge 2.0/3.0.

The AP6606C monitors the CC pin to detect a USB Type-C attach/detach. It is capable providing output voltage of 5V to 15V. The AP6606C implements VBUS detection and discharge for the implementation of compliant connection ports. The protection features include over-voltage (D+/D-, CC1/CC2).

## Pin Assignments

**SP Package (SOP-8 Exposed Pad)**




## Ordering Information

AP6606C

Package Type
SP: SOP-8 (Exposed Pad)

Option Code
Please Reference
Option Code Information

## Features

- VDD Supply Voltage: 3.2V to 6.8V
- Supports USB Type-C and USB PD 3.0 (simplified)
  -- 5V to 15V VBUS Source Only
  -- CC1/CC2 Source Terminator 3A
- Supports HiSilicon Fast Charging Protocol (FCP)
- Supports Qualcomm® Quick Charge™ 2.0/3.0 Class A
- Automatically Selects FCP and QC2.0/3.0 Protocols
- VBUSC Discharge Function
- SOP-8 Exposed Pad Package

## Applications

- Wall-Adapter
- Car Charger
- Power Strip
- USB Power Output Port

**Option Code Information**

| Option Code | 5V | 9V | 12V | 15V | Source Capability |
|---|---|---|---|---|---|
| A | 3A | 2A | 1.5A | - | 18W |
| B | 3A | 2A | 1.5A | 1.2A | 18W |
| D | 3A | 3A | 2.5A | 2A | 30W |
| E | 3A | 3A | 3A | 3A | 45W |

## Typical Application Circuit

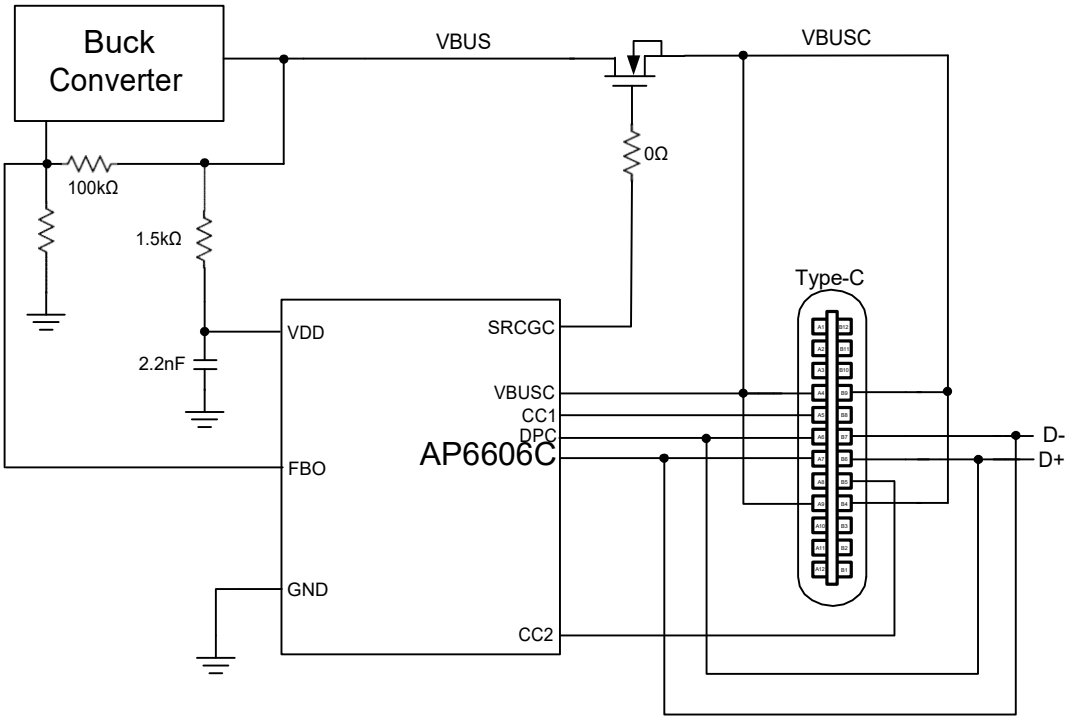
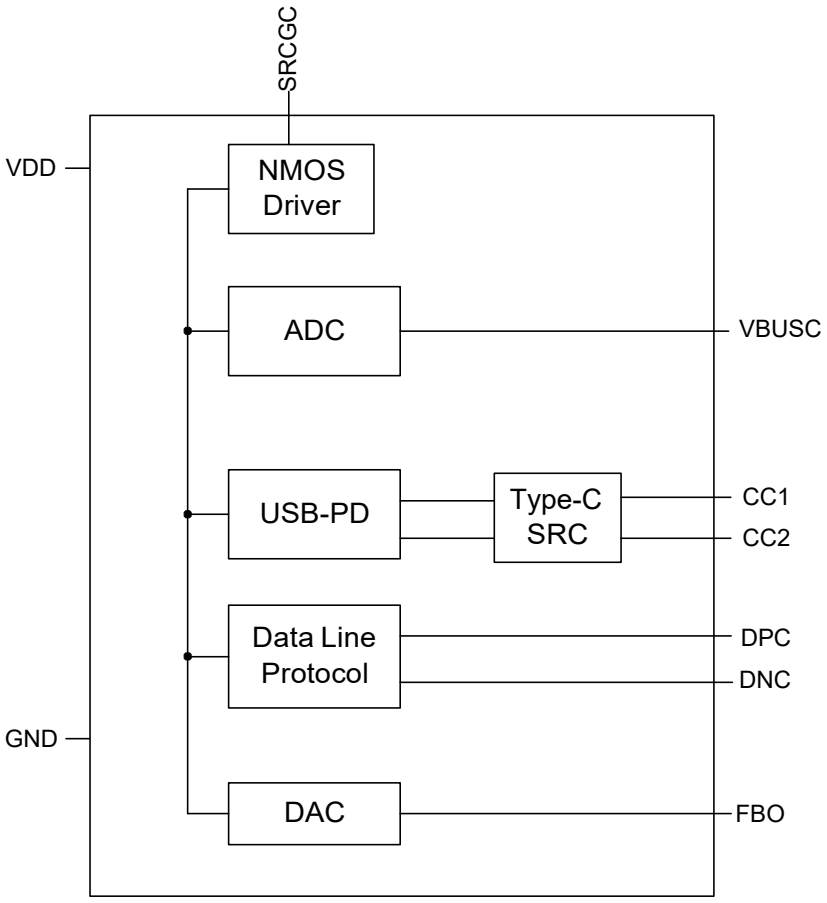



Figure 1. Typical Application Schematic

## Functional Pin Description

| Pin Name | Pin No. | Pin Function |
|---|---|---|
| VDD | 1 | Supply input voltage pin. |
| FBO | 2 | Output voltage control pin. Current sink\source function for FB node. |
| DPC | 3 | USB D+ data line of Type-C. |
| DNC | 4 | USB D- data line of Type-C. |
| CC2 | 5 | USB Type-C Configuration channel signal 2. |
| CC1 | 6 | USB Type-C Configuration channel signal 1. |
| VBUSC | 7 | VBUS voltage discharge function for Type-C connector side. |
| SRCGC | 8 | N-MOSFET gate node control pin. |
| GND | 9 | Ground pin. The exposed pad must be connected to GND and well solder to a large PCB copper area for maximum power dissipation. |

## Block Diagram



## Absolute Maximum Ratings (Note 1)

- Input Supply Voltage VDD ---------- -0.3V to +7V
- DPC, DNC ---------- -0.3V to +18V
- CC1, CC2 ---------- -0.3V to +18V
- SRCGC, VBUSC ---------- -0.3V to +35V
- Maximum Junction Temperature ($T_J$) ---------- +150°C
- Storage Temperature ($T_S$) ---------- -65°C to +150°C
- Lead Temperature (Soldering, 10sec.) ---------- +260°C
- Package Thermal Resistance, ($\theta_{JA}$) (Note 2)

  SOP-8 (Exposed Pad) ---------- 60°C/W
- Package Thermal Resistance, ($\theta_{JC}$)

  SOP-8 (Exposed Pad) ---------- 15°C/W

Note 1: Stresses beyond this listed under “Absolute Maximum Ratings" may cause permanent damage to the device.
Note 2: $\theta_{JA}$ is measured at 25°C ambient with the component mounted on a high effective thermal conductivity test board of JEDEC-51-7.

## Recommended Operating Conditions

- Input supply voltage (VDD) ---------- +3.2V to +6.8V
- Operating temperature range ($T_A$) ---------- -40°C to +125°C
- Junction temperature ($T_J$) ---------- -40°C to +125°C

## Electrical Characteristics

(VDD=5V, $T_A$=25°C and the recommended supply voltage range, unless otherwise specified.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Input Power** | | | | | | |
| VDD Input Voltage Range | $V_{DD}$ | | 3.2 | | 6.8 | V |
| Input UVLO Threshold | $V_{DD\_UVLO}$ | $V_{DD}$ Rising | | 3.3 | | V |
| | $V_{DD\_HYS}$ | $V_{DD}$ Falling | | 2.6 | | V |
| VDD Supply Current | $I_{DD\_SUP}$ | $V_{DD}$ =5V, Nothing Attach | 20 | 33 | 45 | μA |
| VDD Shunt Voltage | $V_{DD\_SHDN}$ | | 5.9 | 6.4 | 6.8 | V |
| **N-MOSFET Gate Driver** | | | | | | |
| SRCGC Sourcing Current | | $V_{DD}$=4V, 0V ≤ $V_{SRCGC}$ – $V_{BUSC}$ ≤ 6V | 4.5 | | 1.8 | μA |
| Sourcing Voltage (ON) between SRCGC and VBUS | | $V_{DD}$=3.2V to 6.8V | 5 | | 15 | V |
| **VBUSC** | | | | | | |
| VBUSC Bleed Discharge Resistance | $R_{\_CBLEED}$ | | 8 | 10 | 12.5 | kΩ |
| VBUSC Discharge Resistance | $R_{\_CDIS}$ | | | 400 | | Ω |
| **USB Type-C** | | | | | | |
| DP/DN OV Threshold (Note 3) | $V_{\_DPDNOV}$ | In QC Mode | | 4 | | V |
| CCOV Rising (Note 3) | $V_{\_CCOV-rising}$ | | | 1.04*$V_{DD}$ | | V |
| CCOV Falling (Note 3) | $V_{\_CCOV-falling}$ | | | $V_{DD}$ | | V |
| **High Voltage Dedicated Charging Port (HVDCP)** | | | | | | |
| Data Detect Voltage | $V_{DAT(REF)}$ | | 0.25 | 0.325 | 0.4 | V |
| Output Voltage Selection Reference | $V_{SEL\_REF}$ | | 1.8 | 2.0 | 2.2 | V |
| DPC High Glitch Filter Time | $T_{GLITCH(BC)-DPA\_H}$ | | 1000 | 1250 | 1500 | ms |
| DNC Low Glitch Filter Time | $T_{GLITCH(BC)-DNC\_L}$ | | | 1 | | ms |
| Output Voltage Glitch Filter Time | $T_{GLITCH(V) CHANGE}$ | | 20 | 40 | 60 | ms |
| DNC Pull-Down Resistance | $R_{DNC(DWN)}$ | | | 20 | | kΩ |
| Continuous Mode Glitch Filter Time | $T_{GLITCH-CONT -CHANGE}$ | | 100 | | 200 | μs |
| DPC Leakage Resistance | $R_{DAT-LKG}$ | $V_{DD}$ =3.2 to 6.4V VDPA=0.6-3.6V Switch SW1=Off | 300 | 500 | 800 | kΩ |
| Switch SW1 On-Resistance | $R_{DS\_ON\_N1}$ | $V_{DD}$ =5V,SW1= 200μA | | | 40 | Ω |
| UP/Down Current Step | $I_{UP}$, $I_{DOWN}$ | $I_{UP}$ = 0μA (5V), 40μA (9V) 70μA (12V), 100uA (15V) $I_{DOWN}$ = 14μA (3.6V) | | 2 | | μA |

## Electrical Characteristics (Continued)

(VDD=5V, $T_A$=25°C and the recommended supply voltage range, unless otherwise specified.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DCP Charging Mode** | | | | | | |
| $DPC_{\_0.48V}$ / $DNC_{\_0.48V}$ Line Output Voltage | | | 0.44 | 0.48 | 0.52 | V |
| $DPC_{\_0.48V}$ / $DNC_{\_0.48V}$ Line Output Impedance | | | | 900 | | kΩ |
| **Apple Mode** | | | | | | |
| $DPC_{\_2.7V}$ / $DNC_{\_2.7V}$ Line Output Voltage | | | 2.57 | 2.7 | 2.84 | V |
| $DPC_{\_2.7V}$ / $DNC_{\_2.7V}$ Line Output Impedance | | | | 33.6 | | kΩ |
| **DNC SECTION (FCP)** | | | | | | |
| DNC FCP Tx Valid Output High | $V_{TX-VOH}$ | | 2.55 | | 3.6 | V |
| DNC FCP Tx Valid Output Low | $V_{TX-VOL}$ | | | | 0.3 | V |
| DNC FCP Rx Valid Output High | $V_{RX-VIH}$ | | 1.4 | | 3.6 | V |
| DNC FCP Rx Valid Output Low | $V_{RX-VIL}$ | | | | 1.0 | V |
| DNC Output Pull-Low Resistance | $R_{PD}$ | | 400 | 500 | 600 | Ω |
| Unit Interval for FCP PHY Communication | UI | $F_{CLK}$ =125kHz | 144 | 160 | 180 | μs |

Note 3: Guarantee by design.

## Function Description

**Data Line Interface (D+/D−)**

AP6606C supports QC 2.0/3.0/FCP protocol on the D+/D− data line. The related registers are assigned to the vendor define registers. When the AP6606C is configured as QC 2.0/3.0/FCP mode, both D+ and D− pin are applied to 2.7V. If sink device has the function of QC 2.0/3.0/FCP, D+ pin will be forced between 0.325V and 2V. In the meanwhile, D+ pin will be automatically connected to D− pin by AP6606C and this process is called the short mode for USB BC1.2 specification. If D+ is continuously applied to the voltage between 0.325V and 2V for 1.25 seconds, the AP6606C will enter QC 2.0/3.0/FCP operation mode. The QC 2.0/3.0 could be classed as the following table.

| D+ | D− | Output Voltage |
|---|---|---|
| 0.6V | 0.6V | 12V |
| 3.3V | 0.6V | 9V |
| 0.6V | 3.3V | Continuous mode |
| 0.6V | High-Z | 5V (Default) |

When the voltage of D+ pin and D− pin simultaneously satisfy these two inequalities VDAT(REF)< D+ < VSEL_REF and D− > VSEL_REF, the AP6606C would enter continuous mode.

In the continuous mode, each voltage pulse on D− pin generated by sink device is between 3V and 1V. At the same time, the low level of pulse should be keep at least 200us (default). If the specified conditions are satisfied, the FBO pin will source 2μA (default) per pulse. The maximum source current is 70μA for output voltage 12V.

If the sink device doesn't support QC 2.0/3.0, thAP6606C will remain default output voltage 5V for safe operation. On the other hand, when USB cable is removed, the voltage of D+ pin is therefore lower than VDAT(REF) and the output default voltage 5V is also applied.

**VBUS Control**

The AP6606C is a controller so that it must be combined with power stage. The FBO pin of AP6606C must be connected to the feedback node of power stage. The VBUS control of AP6606C is implemented by sourcing/sinking current from FBO pin.

**VBUSC Discharge**

When Type-C device plug out connector, N-MOSFET will be turned off. At this moment in time, AP6606C execute VBUSC dischange function to avoid Type-C connector existing remaining voltage. If Type-C connector exist remaining voltage, when device plug in, it maybe damage device.

**Data Line Protection**

When DPC/DNC pin is touched by the external power in abnormal situation, the D+/D- pin of sink device and source device may be damaged. In order to protect the DPC/DNC pin of the devices from damage in abnormal situation, the AP6606C will return the output voltage to default output voltage 5V when the voltage of DPC/DNC pin is higher than 4V.

**Configuration Channel Protection**

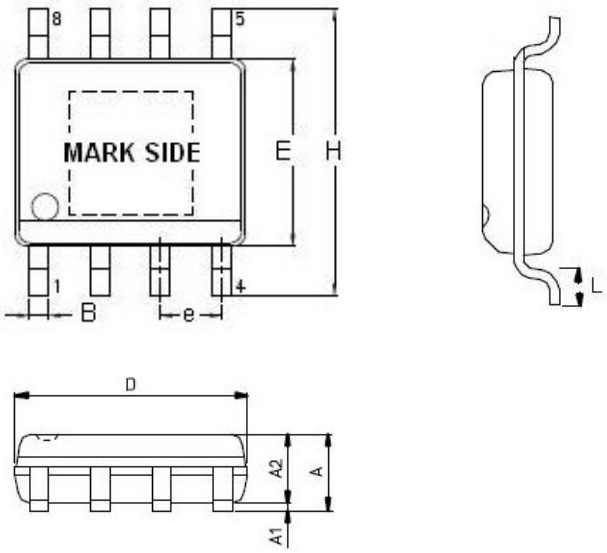
When CC1/CC2 pin is touched by the external power in abnormal situation, the CC1/CC2 pin of both sink device and source device may be damaged. In order to protect the CC1/CC2 pin of the devices from damage in abnormal situation, the AP6606C will return the output voltage to default output voltage 5V.

**Shunt Regulator**

The VDD of AP6606C is supplied by the wide output voltage through the external resistor RVDD. The internal Zener-Diode is utilized to clamp the VDD at 6.8V. The recommended value of RVDD and CVDD are 1.5kΩ and 2.2nF, respectively.

## Outline Information

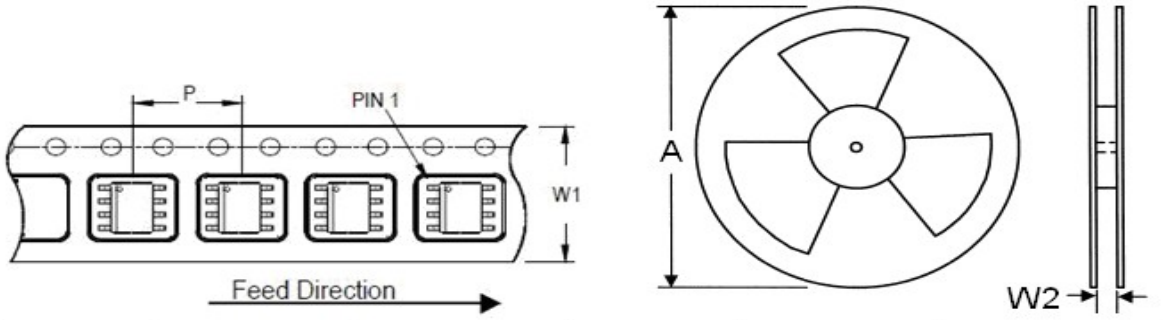
**SOP-8 (Exposed Pad) Package (Unit: mm)**




| SYMBOLS UNIT | DIMENSION IN MILLIMETER | |
|---|---|---|
| | MIN | MAX |
| A | 1.25 | 1.70 |
| A1 | 0.00 | 0.15 |
| A2 | 1.25 | 1.55 |
| B | 0.31 | 0.51 |
| D | 4.80 | 5.00 |
| D1 | 3.04 | 3.50 |
| E | 3.80 | 4.00 |
| E1 | 2.15 | 2.41 |
| e | 1.20 | 1.34 |
| H | 5.80 | 6.20 |
| L | 0.40 | 1.27 |

Note: Followed From JEDEC MO-012-E.

## Carrier Dimensions




| Tape Size (W1) mm | Pocket Pitch (P) mm | Reel Size (A) in | Reel Size (A) mm | Reel Width (W2) mm | Empty Cavity Length mm | Units per Reel |
|---|---|---|---|---|---|---|
| 12 | 8 | 13 | 330 | 12.4 | 400~1000 | 2,500 |